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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/418,663	10/14/1999	James Robert Howard Hakewill	ARGONA.001A	9183

27299 7590 07/16/2003

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EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	16

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/418,663	HAKEWILL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-27,40-42,47,48 and 60-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-27,40-42,47,48 and 60-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *15* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION-Final

Introduction

1. Title is: METHOD AND APPARATUS FOR MANAGING THE CONFIGURATION AND FUNCTIONALITY OF A SEMICONDUCTOR DESIGN.

2. Applicants are: HAKEWILL et al.

3. This action is in response to Applicant's Amendment received 5/23/03. Applicant cancelled claims 1-11, 28-39, 43-46, and 49-59. Applicant amended claims 12, 18, 23, 40, 47, 48, and 60. Applicant added claims 75-78.

4. The pending claims are 12-27, 40-42, 47-48, and 60-78.

5. Applicant claims priority to provisional application 60/104,271 filed Oct. 14, 1998.

6. The interview summary for February 6, 2003 is attached to this action.

7. This is the second action on the merits, and is final.

Index

8. **Dangelo'678** refers to Dangelo et al. US Patent 6,324,678 B1.

9. **Dupenloup'123** refers to Dupenloup et al. US Patent 6,378,123 B1.

10. **Wirthlin'434** refers to Wirthlin et al. US Patent 6,173,434.

11. **Dangelo'958** refers to Dangelo et al. US Patent 5,801,958.

12. **Rostoker'399** refers to Rostoker et al. US Patent 5,867,399.

13. **Cambell** refers to Cambell et al., "A tutorial for make", Proceedings of the 1985 ACM annual conference on the range of computing: mid-80's perspective, 1985, Denver, Colorado, United States. Pages 374-380. ISBN 0-89791-170-9.

14. **Gupte'474** refers to Gupte et al. US Patent 5,903,475.

15. **Heile'369** refers to Heile et al. US Patent 6,321, 369.

16. **Turino'892** refers to Turino et al. US Patent 5,994,892.

17. **Smith** refers to "HDL Chip Design" by Douglas J. Smith, Ninth printing July 2001, minor updates. First Printing June 1996. Doone Publications. ISBN 0-9651934-3-8. pages 1-25.

APPLICANT REMARKS

18. Applicant's Remarks, page 7-12, are specifically addressed below. The format from the prior office action will be retained as much as possible.

Specification-objections-Trademarks-MAINTAINED

19. Remarks page 12. The Applicant has amended the specification at page 13 line 14 from "Wizard TM" to now read simply "Wizard". Note that simply deleting the "TM" does not satisfy MPEP 608.01(v) which states "The relationship between a trademark and the product it identifies is sometimes indefinite, uncertain, and arbitrary. The formula or characteristics of the product may change from time to time and yet it may continue to be sold under the same trademark. In patent specifications, every element or ingredient of the product should be set forth in positive, exact, intelligible language, so that there will be no uncertainty as to what is meant. Arbitrary trademarks which are liable to mean different things at the pleasure of manufacturers do not constitute such language. Ex Parte Kattwinkle, 12 USPQ 11 (Bd. App. 1931)".

20. Applicant should return the "TM", and should define this "Wizard TM" product ("in positive, exact, intelligible language, so that there will be no uncertainty as to what is meant"). The term "Wizard" appears to be a trademarked term, even thought the "TM" has been deleted by amendment.

Claim 12 (amended)-LEVELS OF ABSTRACTION

21. Remarks, page 12. Applicant unpersuasively asserts that that claim 12 (amended) "operates" at a high level of abstraction and that Dangelo'678 is aimed only at lower levels of design abstraction, and further asserts that "output of Applicant's invention would be an input to the invention of Dangelo'678". Emphasis in original.

22. A brief summary of abstraction hierarchy terminology is useful. See Smith's "HDL Chip Design" at FIG 1.1 through 1.4. Smith page 6 states "A top-down design methodology takes the HDL model of hardware, written at a high level of behavioral abstraction (system or algorithmic), down through intermediate levels, to a low (gate or transistor) level; Figure 1.2." Similarly, though in greater detail, the pyramid in Smith FIG 1.2 displays 6 levels of abstraction:

System concept,

algorithm,

Architecture,

RTL (register transfer level),

Gate, and

Transistor.

23. Additionally, the iterative and cyclical use of these levels of abstraction is shown in Smith FIG 1.3, 1.4, and 1.14. Also see Dangelo'678 FIG 2 for iterative and cyclical use.

24. Thus, HDL chip design begins with high levels of abstraction, and then progresses downward to lower levels of abstraction (usually with some iterative and cyclical progression).

25. Similarly, Claim 12 (amended) begins at a high level of abstraction **"editing a [HDL] first file specific to said design",** and progresses to a low level of abstraction **"netlist".** Thus, claim 12 (amended) progresses from high level to low level. Similarly, Dangelo'678 progresses from high level to low level.

26. Dangelo'678 abstract states "**A method for generating structural descriptions of complex digital devices from high level descriptions",** and Column 2 line 46 states "A methodology for deriving a lower-level, physically implementable description, such as a RTL description of the higher level (e.g. VHDL) description), via an intermediate rule-based tool such as Prolog, is disclosed herein".

27. Applicant's characterization of claim 12 (amended) as operating at high levels is not fully accurate, because claim 12 (amended) progresses from high levels to low levels.

28. Thus, Claim 12 (amended) and Dangelo'678 must be interpreted in the view of one skilled in the art. One of ordinary skill in the art of IC design would be intimately familiar with progressing from high levels of abstraction to low levels of abstraction.

29. Additionally, note that one of ordinary skill in the art would be well acquainted with common design techniques such as creating a "new" design by modifying an "old" (fully tested and commercially successful) design. Further, one of ordinary skill would be well acquainted with the iterative and cyclical nature of troubleshooting and/or optimizing integrated circuit designs. Thus, modification and editing of old designs is a common and ubiquitous method of specifying desired behavior for a "new" device, and one of ordinary skill in the art would interpret Dangelo's FIG 2 iterative modifications as disclosing Applicant's term "editing a first file specific to said design". See Dangelo's FIG 2. This discussion also applies to the other amended independent claims: 18, 23, 40, 47, 48, and 60.

30. Remarks page 10. Applicant unpersuasively asserts that that amended independent Claims 23, 40, 47, 48 and 60 are patentable due to the "high level of abstraction". Claims 23

(amended), 40 (amended), 47 (amended), and 48 (amended) have been amended to include the term "high level of abstraction" in the preamble. Claim 60 (amended) has been amended to include the term "high level of abstraction" in one of the limitations. As discussed above with respect to claim 12 (amended), Dangelo'678 discloses "high level of abstraction".

31. New claims 75-78 state "high level of abstraction" in the preambles, and in some of the limitations. As previously discussed, Dangelo'678 discloses "high level of abstraction".

32.

Claim 18 (amended)-CONSTRAINED SET OF DESIGN VARIABLES

33. Applicant Remarks, page 10. Applicant unpersuasively asserts that that the Claim 18 (amended) limitation "input relating to a constrained set of design variables" is distinguished from Dangelo'678 and Dupenloup'123. Specifically, Applicant asserts "such constraints provide the user/designer with a "box of parts" which are known to work together and interact with the design basis (for example, the base case processor core) in predictable and stable manner."

34. Dangelo'678 states at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL". Thus, Dangelo'678 "desired behavior of the device" discloses Claim 18 (amended) "input relating to a constrained set of design variables".

35. Note that Applicant's interpretation of the term "constrained set of design variables" as providing the user/designer with a "box of parts" is not supported by Claim 18 (amended). From the Specification as a whole, and in view of Applicant's characterization of Claim 18 (amended), it appears that the Applicant may intend to provide certain specific known and tested components to be used as building blocks to create the design. Alternately, possibly the Applicant may intend that the design should interface with certain specific known and tested components.

36. The Applicant's intentions are not clear. However, the claim language is clear and very broad. Claim 18 (amended) limitation **"input relating to a constrained set of design variables"** is disclosed by Dangelo'678 Column 3 line 49 **"First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".**

Claim Rejections - 35 USC § 112- first paragraph- enablement-WITHDRAWN

37. The prior objections are withdrawn due to Applicant's amendments, and persuasive assertions at Remarks pages 10-12.

Claim Rejections - 35 USC § 112- fourth paragraph- further limitation-MOOT

38. Applicant has cancelled all claims that were rejected under 35 USC 112 fourth paragraph (further limitations) thus rendering said rejections moot.

Claim Rejections - 35 USC § 102(e)-MOOT

39. Applicant has cancelled all claims that were rejected under 102(e), thus rendering the prior 102(e) rejections moot.

Claim Interpretation

40. LABELS. Note that some of the claims have many limitations. The Examiner has labeled some of these limitations for the sake of clarity.

41. PARENTHETICAL EXPRESSIONS. Applicant has omitted parenthetical expressions such as "(amended)" and "(new)" from the amended and new claims. See 37 CFR 1.121(c)(1)(i). The Examiner will refer to these amended and new claims using parenthetical expressions. Please use the appropriate parenthetical expressions in future correspondence.

Claim Rejections - 35 USC § 103

42. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

43. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> Determining the scope and contents of the prior art.
> Ascertaining the differences between the prior art and the claims at issue.
> Resolving the level of ordinary skill in the pertinent art.
> Considering objective evidence present in the application indicating obviousness or nonobviousness.

44. Claims 12-27, 40-42, 47-48, and 60-78 are rejected under 35 U.S.C. 103(a) as being unpatentable.

45. Claim 12 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

46. Claim 12 is in independent claim with 8 limitations.

47. A-**editing a first file specific to said design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.

48. B-**defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

49. C-**generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

50. D-**running said script to create said customized description language model** is disclosed by Dangelo at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

51. E-**generating a netlist which is descriptive of the circuitry of said integrated circuit** is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".

52. F-**compiling said netlist and said hardware description model to produce a compiled integrated circuit design** is disclosed by Dangelo'678 at Column 49 line 56 "compiling and simulating the netlist".

53. G-**fabricating at least one mask representing said compiled integrated circuit design** is disclosed by Dangelo'678 at Column 41 line 59 "mask level".

54. I-**wherein said act of creating is performed at a high level of abstraction is disclosed** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL". Note that Applicant's term "creating" refers to limitations A-D, which are inherently performed at a high level of abstraction. This limitation may be redundant.

55. Dangelo'678 does not expressly disclose "fabricating said integrated circuit using said at least one mask".

56. H-**fabricating said integrated circuit using said at least one mask** is disclosed by Dupenloup'123 at Column 79 line 66 "wafer corresponding to the pattern on the mask".

57. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenlup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this fabricate the design that Dangelo'678 produced, because optical masks and photoresist on silicon wafers is the standard way to produce integrated circuits. Although Dangelo'678 does not explicitly discuss fabrication, it is implicit that Dangelo's IC design will be fabricated according to standard methods (after simulation testing and so forth).

58. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

59. Claim 13 depends from Claim 12 (amended), with four additional limitations.

60. **(ii)cache configurations** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more randam access memories (RAM) 830").

61. **(iii)memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

62. **(iv)system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

63. Dangelo'678 does not expressly disclose custom instruction sets.

64. (i)custom instruction sets is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

65. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to fabricate the design that Dangelo'678 produced.

66. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

67. Claim 14 depends from Claim 12 (amended), one additional limitations.

68. **generating a list of logic devices and their interconnections** is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".

69. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

70. Claim 15 depends from Claim 12 (amended), with one additional limitation.

71. Dangelo does not expressly disclose lithographic process.

72. **defining physical features on a semi-conductive substrate via a lithographic process** is disclosed by Dupenloup'123 at Column 79 line 58 to Column 80 line 1 "Photolithography...semiconductor material".

73. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678 produced.

74. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

75. Claim 16 depends from Claim 12 (amended), with one additional limitation.

76. **synthesizing said design based on said description language model** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

77. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Dangelo'958.

78. Claim 17 depends from Claim 13, with one additional limitation.

79. **editing is performed interactively with the user using a display** is disclosed by Dangelo'958 at Column 10 line 45 "user input occurs by pointing with the pointing device and selecting connection nodes, nets or devices and issuing commands which affect the selected object's numerical parameters". Note that Dangelo'958 "point and select" inherently discloses: a display, a pointer, and related graphical user interface software. Dangelo's "point and select" precisely discloses interactive editing, where the user interacts with a display using a pointer and related software.

80. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Dangelo'958 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678

produced, and to facilitate the user interaction with the editing program. Graphical user interfaces including "point and click" menus are universally recognized as efficient ways to interact with computers. For example, graphical user interfaces including a pointing mouse and clicking menus have been standard even on cheap personal computers for approximately 8 years.

81. Claim 18 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

82. Claim 18 (amended) is an independent "apparatus" claim with 7 limitations.

83. D-**a computer program resident at least in part on said storage device, said computer program adapted to receive said input relating to a constrained set of design variables from said user and perform the following acts on said input: editing a first file specific to said integrated circuit design** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

84. E-[a computer program resident...] **defining the location of at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

85. F-[a computer program resident...] **generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

86. G-[a computer program resident...] **running said script to create said description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

87. Dangelo'678 does not expressly disclose processor, storage device, and input device.

88. A-**a processor capable of running a computer program** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.

89. B-**a storage device being capable of storing at least a portion of a computer program** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

90. C-**an input device, operatively coupled to said processor, capable of receiving input from a user and transmitting said input to said processor** is disclosed by Dupenloup'123 at FIG 46 element 964 INPUT DEVICE.

91. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

92. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

93. Claim 19 depends from Claim 18 (amended), with one additional limitation.

94. said description language model is a hardware description language (HDL) is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

95. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

96. Claim 20 depends from Claim 18 (amended), with two additional limitations.

97. **generating a second file based on said description language model for use with a simulation** is disclosed by Dangelo'678 at Column 1 line 53 "information necessary for layout, verification and simulation into a schematic object file or files".

98. simulating said design using said second file is disclosed by Dangelo'678 at Column 1 line 61 "generates a set of simulation results".

99. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

100. Claim 21 depends from Claim 20, with one additional limitation.

101. running synthesis scripts based on said description language model in order to synthesize said integrated circuit design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

102. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

103. Claim 22 depends from Claim 18 (amended), with two additional limitations.

104. Dangelo'678 does not expressly disclose digital microprocessor and magnetic media storage device.

105. **said processor comprises a digital microprocessor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.

106. **said storage device comprises magnetic media** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

107. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

108. Claim 23 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

109. Claim 23 is an independent "system" claim with six limitations.

110. B-**a first file comprising at least one instruction** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".

111. C-**a second file comprising a plurality of cache configurations** is disclosed by is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions".

112. D-**a third file comprising a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

113. E-**a second algorithm capable of generating a script based on selections made by said user from said first, second, and third files and**

114. **input to said computer program via said input device** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

115. F-**a third algorithm capable of running said script to generate a description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

116. Dangelo'678 does not expressly disclose a computer having a processor and an input device.

117. A-**a computer having a processor and an input device** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR and element 964 INPUT DEVICE.

118. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

119. As discussed (in substantial detail) above with respect to claim 12 (amended), Dangelo'678 discloses "high level of abstraction".

120. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Rostoker'399.

121. Claim 24 depends from Claim 23 (amended), with two additional limitations.

122. Dangelo'678 does not expressly disclose object code and storage device.

123. said program is embodied in object code is disclosed by Rostoker'399

124. stored on a storage device accessible by said processor is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

125. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 and Rostoker'399 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

126. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Rostoker'399.

127. Claim 25 depends from Claim 24, with one additional limitation.

128. Dangelo'678 does not expressly disclose "rotating media magnetic storage device".

129. **rotating media magnetic storage device** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE and Column 76 line 40 "such as a disk drive unit".

130. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 and Rostoker'399 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors.

131. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

132. Claim 26 depends from Claim 23 (amended), with one additional limitation.

133. fourth file comprising a plurality of system architectures is disclosed by Dangelo'678 at Column 2 line 31 "VHDS supports three distinct styles for the description of hardware architectures".

134. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

135. Claim 27 depends from Claim 23 (amended), with one additional limitation.

136. **fourth algorithm capable of simulating said integrated circuit design based on said description language model** is disclosed by Dangelo'678 at Column 1 line 47 "logic simulator".

137. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

138. Claim 40 is an independent "system" claim (or "machine" per 35 USC 101), with 8 limitations.

139. **4-(ii) a plurality of cache configurations** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

140. **5-(iii) a plurality of memory interface configurations** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

141. Dangelo does not expressly disclose "custom instruction".

142. **6-(iv) a plurality of system architecture configurations** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

143. 7-a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

144. **8-a second algorithm capable of running said script to generate a description language model of an integrated circuit design** is disclosed by Dangelo'678 at Column 14 line

20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

145. Dangelo'678 does not expressly disclose limitations 1-3.

146. **1-a processor** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR

147. **2-a storage device in data communication with said processor** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM.

148. **3-(i) a plurality of custom instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

149. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36.

150. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and Gupte.

151. Claim 41 depends from Claim 40, with one additional limitation.

152. Dangelo'678 does not expressly disclose the additional limitation.

153. **plurality of process technology options** is disclosed by Gupte at Column 4 line 60 "process technology".

154. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to do this to save time and money by using the same circuit design methods for different process technologies.

155. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434 and official notice (and mere automation).

156. Claim 42 depends from Claim 40, with one additional limitation.

157. Dangelo'678 does not expressly disclose the additional limitation.

158. **pre-configured data file** is disclosed by official notice that it is well known in the art to store the detailed parameters of user selected elements in pre-configured data files.

159. Also, using pre-configured data files is **merely automating** the manual entry of said data. In re Venner, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art."

160. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Dupenloup'123 and Wirthlin'434 and official notice of data files to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to implement the procedure of Dagngelo'678 using the processor of Dupenloup'123, and to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to allow the user to quickly and accurately input large amounts of data in the form of pre-configured data files.

161. Claim 47 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

162. Claim 47 (amended) is an independent "method" claim with 9 limitations.

163. **3-(ii) cache configuration** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

164. **4-(iii) memory interface configuration** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

165. **5-(iv) system architecture configuration** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

166. 6-defining the location of at least one library file is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

167. **7-generating a script using said first file and said library** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

168. 8-running said script to create a customized hardware description language model of the design is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

169. **9-running a synthesis algorithm to synthesize a file descriptive of said design** is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".

170. Dangelo'678 does not expressly disclose 2 of the limitations.

171. **1-selecting a process technology** is disclosed by Gupte at Column 4 line 60 "process technology".

172. 2-(i) processor instructions is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

173. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to use Gupte to save time and money by using the same design program for various technologies, and to use Wirthlin'434 to save time by customizing the clock cycles to match the level of complexity of the instructions.

174. Claim 48 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123 and Wirthlin'434.

175. Claim 48 (amended) is an independent "means for" claim with substantially the same limitations as Claim 40, thus is rejected for the same reasons.

176. Claim 60 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

177. Claim 60 (amended) is an independent method claim with 2 limitations.

178. **generating, at a high level of abstraction, a description of a hardware implementation of said configurable processor** is disclosed by Dangelo'678 at Column 14 line

20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

179. Dangelo'678 does not expressly disclose one limitation:

180. at least one user-defined instruction is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

181. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

182. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

183. Claim 61 depends from Claim 60 (amended), with one additional limitation.

184. Dangelo'678 does not expressly disclose the additional limitation:

185. **generating a description including control logic necessary for the execution of said at least one user-defined instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

186. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

187. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

188. Claim 62 depends from Claim 61, with one additional limitation.

189. **instruction execution pipeline having a plurality of stages, said control logic including portions associated with said stages** is disclosed by Dangelo'678 at Column 27 line 22 "specific control elements are assigned to the control logic in the RT level description of the system".

190. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434 and Turino'892.

191. Claim 63 depends from Claim 60, with 3 additional limitations.

192. **(i)-registers** is disclosed by Dangelo'678 at Column 7 line 29 "registers".

193. **(iii)-scratchpad RAM** is disclosed by Dangelo'678 at Column 11 line 60 "RAM".

194. Dangelo does not disclose one limitation:

195. **(ii)-condition code choices** is disclosed by Turino'892 at Column

196. "Condition Code Register (CCR) - - 8 bits".

197. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Turino'892 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to minimize the number of bits in the condition code register.

198. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

199. Claim 64 depends from Claim 60, with 1 additional limitation.

200. **at least one library of multimedia extensions** is disclosed by Dangelo'678 at Column 9 line 2 "libraries".

201. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

202. Claim 65 depends from Claim 60, with 1 additional limitation.

203. **simulating said configurable processor** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

204. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

205. Claim 66 depends from Claim 65, with 3 additional limitations.

206. **running at least one script to generate simulation data** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

207. **running at least one simulation using at least said simulation data** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

208. determining the adequacy of said configurable processor based at least in part on said act of running is disclosed by Dangelo'678 at Column 4 line 18 "This provides a check that the circuit implementation behaves as intended, and that the timing goals are achieved.

209. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

210. Claim 67 depends from Claim 60, with 1 additional limitation.

211. synthesizing said configurable processor using at least said description is disclosed by Dangelo'678 at Column 4 line 6 "synthesis".

212. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

213. Claim 68 depends from Claim 67, with 2 additional limitations.

214. **running at least one synthesis script to generate synthesis data** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

215. evaluating the adequacy of said synthesis data based at least in part on at least one design criterion is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

216. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

217. Claim 69 depends from Claim 68, with 2 additional limitations.

218. at least one processor die size criterion is disclosed by Dangelo'678 at Column 41 line 46 "die size".

219. Dangelo'678 does not expressly disclose one limitation:

220. at least one specific processor performance criterion is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

221. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

222. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

223. Claim 70 depends from Claim 68, with 3 additional limitations.

224. **revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

225. re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

226. and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

227. Claim 71 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

228. Claim 71 depends from Claim 70, with 2 additional limitations.

229. **at least one processor die size criterion** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

230. **revising at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

231. Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

232. Claim 72 depends from Claim 71, with 2 additional limitations.

233. **at least one processor die size criterion** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

234. **revising at least one control file** is disclosed by Dangelo'678 at Column 27 line 22 "control elements".

235. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

236. Claim 73 depends from Claim 70, with 2 additional limitations.

237. **processor clock speed** is disclosed by Dangelo'678 at Column 10 line 52 "length of clock cycle"

238. **at least one library** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

239. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

240. Claim 74 depends from Claim 70, with 2 additional limitations.

241. **processor power consumption** is disclosed by Dangelo'678 Column 19 line 47 "allows the user to perform a "what if" analysis for choosing a preferred design in terms of size, speed, performance, technology, and power".

242. **at least one netlist (net load)** is disclosed by Dangelo'678 Column 49 line 56 "compiling and simulating the netlist".

243. Claim 75 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte.

244. Independent claim 75 (new) is a method claim with 8 limitations.

245. A-**providing an existing core configuration** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints". Also see Dangelo'678 FIG 2 which illustrates the iterative nature of integrated circuit design.

246. B-**editing a first file specific to the design, said editing comprising selecting a constrained set of input parameters associated with said configuration, said parameters comprising: (i)at least one custom instruction** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line", and at Column 14 line 21 "dc-shell script and constraints files", and at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.

247. E-**providing at least one library file** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

248. F-**generating a script using said first file, said library file, and user input information** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

249. G-**running said script to create a customized description language model** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

250. H-**synthesizing said design based on said description language model** is disclosed by Dangelo'678 Column 49 line 56 "compiling and simulating the netlist".

251. Dangelo does not expressly disclose the additional limitations.

252. C-**(ii)a cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

253. D-**(iii) a memory interface configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

254. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to select cache configurations and memory interface configurations in order to customize the process of Dangelo'678 to quickly and cheaply design alternate combinations of configurations and instructions, and to increase the overall circuit performance speed by inserting a cache memory as a buffer.

255. Claim 76 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte.

256. Independent claim 76 (new) is a method claim with 7 limitations.

257. E-**generating a script based on said at least one optional instruction, cache instruction, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

258. F-**running said script to generate a hardware description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

259. Dangelo does not expressly disclose the additional limitations.

260. A-**providing a user with a plurality of optional instructions, including the ability to generate a customized instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

261. B-**selecting at least one of said plurality of optional instructions** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

262. C-**selecting at least one cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

263. D-**defining at least one memory interface** is disclosed by Gupte at Column 6 line 18 "cache memory".

264. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to apply Dangelo'678 design methods to cache memories to speed processing.

265. Claim 77 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

266. Independent claim 77 (new) is a method claim with 7 limitations.

267. E-**generating a script based on said at least one optional instruction, cache configuration, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

268. F-**running said script to generate a hardware description language model of said integrated circuit design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

269. Dangelo'678 does not explicitly disclose the additional limitations.

270. A-**editing a first file specific to said integrated circuit design including selecting a plurality of input parameters associated with said design, said parameters comprising: (i) at least one custom instruction set** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

271. B-**(ii) a cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

272. C-**selecting at least one cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

273. D-**defining at least one memory interface** is disclosed by Gupte at Column 6 line 18 "cache memory".

274. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to apply Dangelo'678 design methods to cache memories to speed processing.

275. Claim 78 (new) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.

276. Independent claim 78 (new) is a method claim with 7 limitations.

277. E-**generating a script based on said at least one optional instruction, cache configuration, and memory interface** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

278. F-**running said script to generate a hardware descriptive language model of said processor design** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

279. Dangelo'678 does not explicitly disclose the additional limitations.

280. A-**providing the user with a basecase processor configuration having a base instruction set** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

281. B-**providing a user with a plurality of optional instructions adaptable for use with said basecase core** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

282. C-**selecting at least one cache configuration** is disclosed by Gupte at Column 6 line 18 "cache memory".

283. G-**wherein said plurality of optional and cache configurations are constrained so as to ensure the functionality of said processor design irrespective of the user's selection** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

284. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to apply Dangelo'678 design methods to cache memories to speed processing.

Conclusion

285. All pending claims are rejected under 35 USC 103.

Response to Amendments or new IDS-FINAL OFFICE ACTION

Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:
(703) 746-7238 --- for communications after a Final Rejection has been made;
(703) 746-7239 --- for other official communications; and

(703) 746-7240 --- for non-official or draft communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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